The Design of Active Floating Positive and Negative Inductors in MMIC Technology

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Abstract—**An original method for the determination of all possible inductive circuits as a function of the number of FET's used is described in this paper. The method is of general use in monolithic microwave integrated circuits. Circuits with large inductance, either positive or negative in value, can be obtained along with low loss or even negative resistance.**

I. Introduction

One of the major limitations in the design of the GaAs MMIC is the difficulty in realizing low loss spiral inductors with values greater than 2 nH. The most promising solution seems to be with active inductors [1]–[3]. We propose an original method that permits the determination of all possible inductive circuits as a function of the number of FET's used. The circuits have high inductance, and both positive and negative values of inductance have been obtained. Low loss can also be obtained with the possibility of negative resistance as well. Their Y admittance is equivalent to that of a parallel $R_m L_m C_m$ circuit.

II. Active Inductors with Low Loss

Assume the FET's can be represented only by a transconductance g_m and the gate-source capacitance C_{gs}. The study of all circuits, having two FET's each, shows the existence of two positive inductive circuits (Fig. 1). Those circuits are called positive elementary cells. The same study shows also the existence of two other negative inductive circuits (Fig. 2), also called negative elementary cells. Notice the augmentation of C_{gs2}, by the addition of a capacitance (C) between the gate and the T2 source (Figs. 1 and 2), leading to an increase of the inductance. However, the problem becomes more complicated when we replace each FET by its complete model (C_{gs}, g_m, C_{gd}, C_{ds} and g_d). In this case, the capacitance (C) can vary slightly the capacitance C_m and the resistance R_m of the equivalent circuit. The simple analysis is adequate for describing how the inductance is obtained. However, realistic circuits must include bias circuitry and other parasitics, and a complete analysis can only be obtained with computer simulation.

We notice that the rule governing the evolution of the inductive circuits from the elementary cells can be summed up by adding a FET in the beginning, middle or end of the elementary cell following the schematic shown in Figs. 3 and 4. Their Y admittance is equivalent to that of a parallel $R_m L_m C_m$ circuit. Only three of these 12 circuits have already been published. A four FET inductor can be conceived by adding a combination of two among these three forms of the FET on the elementary cells. A five-FET inductor can be conceived by adding a combination of three and so and so forth.

The study of these floating active inductors, with three FET's, shows that in general their equivalent RLC circuit creates a larger inductor with a higher resistor. The calculus of admittance shows that adding a supplementary capacitance

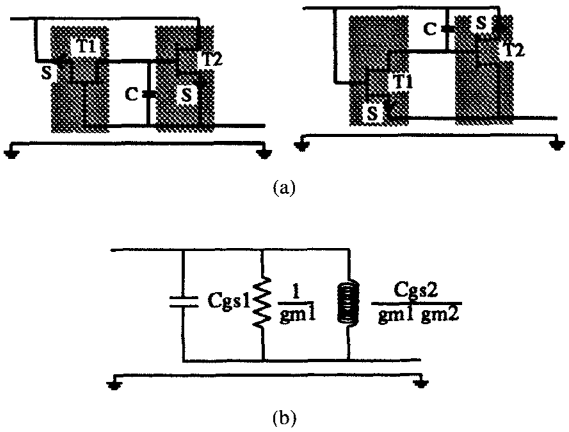

Fig. 1. Elementary cells of the floating positive active inductors. (a) Circuit configuration. (b) Equivalent circuit.

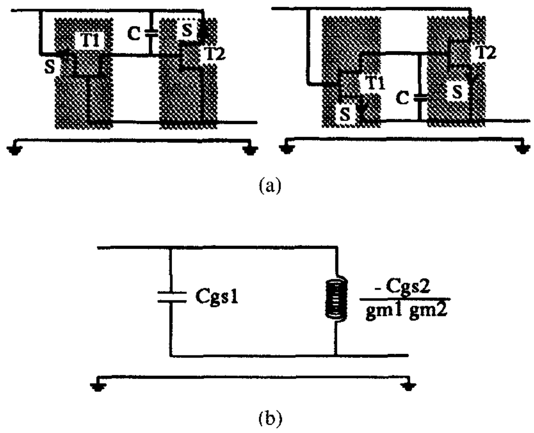

Fig. 2. Elementary cells of the floating negative active inductors. (a) Circuit configuration. (b) Equivalent circuit.

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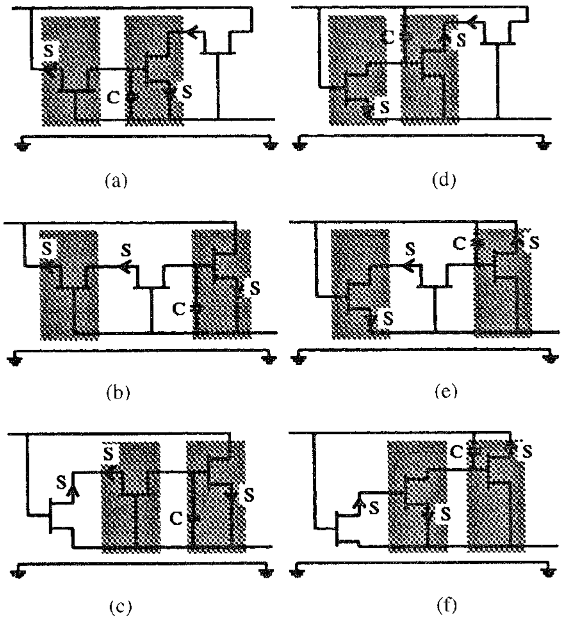

Fig 3 Circuit configurations of the floating active positive inductor, with three FET's. (a) *IEEE Trans Microwave Theory Tech*, 1989. (b) *Electron. Lett.*, 1991. (c) New. (d) New (e) *IEEE Microwave and Guided Wave Lett.*, 1993 (f) New.

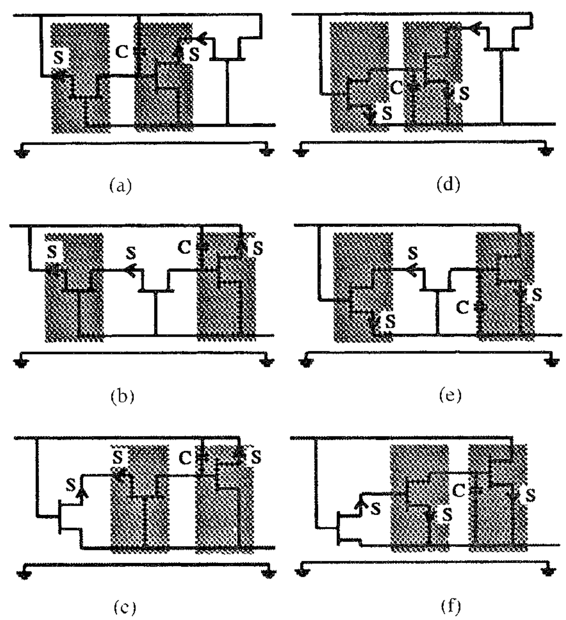

Fig. 4. Circuit configurations of the floating active negative inductor, with three FET's. (a)–(f) New

(C') between the gate and the source of the second FET of the elementary cell introduces in the equivalent circuit a supplementary inductance—whatever the position of that FET in the circuit. Table I and II display the influence of the capacitance C on the values of L_m, C_m and R_m of the equivalent circuit of the inductive circuits containing three FET's, after having replaced each FET by its complete model, when $g_m = 5.36$ mS, $C_{gs} = 0.0522$ pF, $C_{ds} = 8.9$ fF, $C_{gd} = 8$ fF, $g_d = 0.5$ mS (when 40 μm gate-width FET's are used). The MMIC technology used is a 0.7 μm one, from Philips Microwave, with an intrinsic cut-off frequency

TABLE I
INFLUENCE OF THE CAPACITANCE C ON THE L_m, R_m, AND C_m FOR EQUIVALENT CIRCUIT OF THE ACTIVE POSITIVE INDUCTOR

		Lm (nH)	Cm (pF)	Rm (Ohm)
Fig 3.a	C=0	3,5	0,08	≤300
	C=0,448 pF	20	0,08	185
Fig 3.b	C=0	3	0,08	≤300
	C=0,448 pF	18	0,085	180
Fig 3.c	C=0	5	0,055	≤1000
	C=0,448 pF	36	0,055	1400
Fig 3.d	C=0	4	0,075	≤1 k
	C=0,448 pF	25	0,06	≤700
Fig 3.e	C=0	3	0,09	≤600
	C=0,448 pF	19	0,07	≤400
Fig 3.f	C=0	3	0,06	≤300
	C=0,448 pF	20	0,05	≤350

TABLE II
INFLUENCE OF THE CAPACITANCE C ON THE L_m, R_m, AND C_m FOR EQUIVALENT CIRCUIT OF THE ACTIVE NEGATIVE INDUCTOR

		Lm (nH)	Cm (pF)	Rm (Ohm)
Fig 4.a	C=0	-3,5	0,08	≥300
	C=0,448 pF	-20	0,08	≥500
Fig 4.b	C=0	-2,5	0,075	-∞ +∞
	C=0,448 pF	-18	0,1	700
Fig 4.c	C=0	-6	0,06	≥10k et <0
	C=0,448 pF	-42	0,062	-600
Fig 4.d	C=0	-3,5	0,06	≥0 et ≤0
	C=0,448 pF	-21	0,07	≥1,5k
Fig 4.e	C=0	-3,5	0,06	≤300
	C=0,448 pF	-20	0,075	800
Fig 4.f	C=0	-4	0,05	1k
	C=0,448 pF	-22	0,05	≥1k

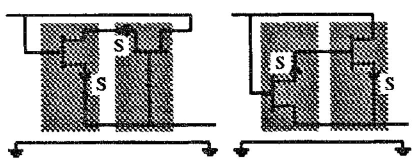

Fig. 5. Other inductive positive inductors containing two FET's giving large losses and weak inductance.

$f_T = g_m/2\pi C_{gs}$ of 20 Ghz at $I_{DSS}/2$. The simulation results presented in Table I and II were obtained with Academy (Eesof trade mark) for the following operating condition, $I_{DS} = I_{DSS}/2$ and $V_{DS} = 3$ V.

III. ACTIVE INDUCTORS WITH LARGE LOSSES

The study of the two FET circuits also shows the existence of two positive inductors (Fig. 5). Their inductance (L_m) is weaker and the losses are more important when compared to the losses in the elementary cells. The inductive circuits (with n FET's) generated from those circuits according to the same designing rule also represent a weaker inductance than those of the inductive circuits generated from the elementary positive cells, as well as the most important losses. The study of circuit at two FET's also shows the existence of two negative inductive circuits, having smaller inductance, and more important losses than those of the negative elementary cells. The circuits generated from these possess the same properties. Thus, inductors with large losses can be obtained if a FET in common drain is added at the end of each elementary cell or another elementary cell.

IV. Conclusion

We have proposed an original method for the determination of all possible inductive circuits as a function of the number of FET's used. The higher values obtained for the inductor, already well known and well masterd by designers in the low frequency field, opens the door to direct application in the field of microwave synthesis methods.

References

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